UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,803	11/04/2003	Masahiro Yoshida	1248-0677P	4032

2292 7590 01/09/2007

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/09/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/699,803	YOSHIDA, MASAHIRO	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 October 2006 has been entered. Claims 1-20 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al. (US 2004/0021616) in view of Kawaguchi et al. (US 6,677,925).

Regarding claims 1, 6 and 7, Goto et al. disclose an active matrix substrate, a display comprising an active matrix substrate and a display comprising display panels each including an active matrix substrate (Figure 1) comprising:

first bus lines and second bus lines arranged to form a matrix (Figure 1 shows first bus lines DL1 through DLn+2 and second bus lines GL1-1 through GL1-m and GL2-1 through GL2-k.);

switching devices provided near respective intersections of the first bus lines and the second bus lines (Figure 1 shows switching devices 10 provided at the intersections of the first and second bus lines.); and

pixel electrodes electrically connected to the first bus lines and the second bus lines through the switching devices (Figure 1 shows pixel electrodes 12 that are connected to the first and second bus lines through transistor 10.), wherein:

at least one of the first bus lines has a first capacitance formed thereon (Figure 1 shows that first bus lines DLn+1 through DLn+2 have a capacitance formed on them by capacitance adjustment means 24 as explained in paragraph [0061].); and

the first bus lines, except for the at least one first bus line with a first capacitance, are connected to first bus lines on another active matrix substrate (Figure 1 shows that the first bus lines DL1 through DLn are all connected to first bus lines DL1 through DLn on the display 200.).

Goto et al. fail to teach that the capacitance is formed by arranging (i) a first bus line not connected to first bus lines on another active matrix substrate and (ii) a line other than the second bus lines to cross each other.

Kawaguchi et al. disclose of forming a capacitance by arranging a first bus line and a line other a second bus line to cross each other (Figure 1 shows that the first bus lines SL1 through SLn cross a line 12 that is not one of the second bus lines GL1 through GLm, and that a capacitance is formed by crossing these lines as explained in column 8, lines 9-15.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the capacitance adjustment means taught by Goto et al. have the configuration as taught by Kawaguchi et al. such that the capacitance would be formed by two lines crossing each other in order to provide a capacitance adjustment that does not result in a remarkable increase in the number of steps of the manufacturing process.

Regarding claim 2, Goto et al. and Kawaguchi et al. disclose the active matrix substrate as set forth in claim 1.

Goto et al. also disclose wherein the at least one first bus line is connected to a line connected to no pixel electrode on the other active matrix substrate (Figure 1 shows that first bus lines DLn+1 through DLn+2 are connected to lines GL1-1 through GL1-m which are not connected to pixel electrodes on the other matrix substrate on display 200.).

Regarding claim 3, Goto et al. and Kawaguchi et al. disclose the active matrix substrate as set forth in claim 1.

Goto et al. also disclose wherein each of those first bus lines which have no first capacitance formed thereon has a second capacitance formed thereon which is less than the first capacitance (Paragraph [0061] explains that a capacitance is added to lines DLn+1 and DLn+2, which is a first capacitance, because the other lines DL1 through DLn are connected to panel 200 which cause a capacitance to be formed on these lines.).

Regarding claim 4, Goto et al. and Kawaguchi et al. disclose the active matrix substrate as set forth in claim 1.

Goto et al. also disclose wherein the first bus lines are connected to a source driver, and the second bus lines are connected to a gate driver (Figure 1 shows drive circuit 50 which is the gate and source driver as explained in paragraph [0056].).

Regarding claim 5, Goto et al. and Kawaguchi et al. disclose the active matrix substrate as set forth in claim 1.

Goto et al. also disclose wherein the first bus lines are connected to a gate driver, and the second bus lines are connected to a source driver (Figure 1 shows drive circuit 50 which is the gate and source driver as explained in paragraph [0056].).

Regarding claim 8, this claim is rejected under the same rationale as claim 3.

Regarding claim 9, this claim is rejected under the same rationale as claim 4.

Regarding claim 10, this claim is rejected under the same rationale as claim 5.

Regarding claim 11, Goto et al. and Kawaguchi et al. disclose the display as set forth in claim 7.

Goto et al. also disclose wherein one of the display panels is designated as a main panel (Figure 1 and paragraph [0050] explain that the first display panel 1 is used as a main panel.).

Regarding claim 12, please refer to the rejection of claims 1, 6 and 7, and Goto et al. furthermore disclose wherein:

the first bus lines are shared for use among the display panels (Figure 1 shows that lines DL1 through DLn of the first bus lines are shared between panels 1 and 200.);

in at least one of the display panels, at least one of the first bus lines is connected to none of the pixel electrodes on the active matrix substrate (Figure 1 shows that lines DLn+1 and DLn+2 are not connected to pixel electrodes on panel 200.); and

the at least one first bus line connected to none of the pixel electrodes has a first capacitance formed thereon (Figure 1 shows that first bus lines DLn+1 through DLn+2 have a capacitance formed on them by capacitance adjustment means 24 as explained in paragraph [0061].).

Regarding claim 13, this claim is rejected under the same rationale as claim 3.

Regarding claim 14, this claim is rejected under the same rationale as claim 4.

Regarding claim 15, this claim is rejected under the same rationale as claim 5.

Regarding claim 16, this claim is rejected under the same rationale as claim 11.

Regarding claims 17-20, Goto et al. and Kawaguchi et al. disclose the active matrix substrates as set forth in claims 1, 6-7 and 12.

Goto et al. also disclose wherein an amount of the first capacitance is such that there is substantially no difference in signal delay on each first bus line of the active

matrix substrate that is connected to a first bus line on the other active matrix substrate and signal delay on the at least one first bus line with a first capacitance (Paragraph [0061] explains that since the lines not connected to panel 200 are shorter and have less capacitance, that capacitance adjustment must be made to these lines, which would obviously be done to avoid a signal delay.).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

29 December 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER